A High Step-Down Transformerless Single-Stage Single-Switch AC/DC Converter

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Abstract—This paper presents a high step-down transformerless single-stage single-switch AC/DC converter suitable for universal line applications (90–270 Vrms). The topology integrates a buck type power factor correction (PFC) cell with a buck-boost DC/DC cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost type PFC cell, the main switch of the proposed converter only handles the peak inductor current of DC/DC cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results.

Index Terms—Direct power transfer (DPT), integrated Buck-Buck–Boost converter (IBuBuBo), power factor correction (PFC), single-stage (SS) and transformerless.

I. INTRODUCTION

SINGLE-STAGE (SS) AC/DC converters have received much attention in the past decades because of its cost effectiveness, compact in size and simple control mechanism. Among existing SS converters, most of them are comprised of a boost PFC cell followed by a DC/DC cell for output voltage regulation [1]–[7]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high line application [8]. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost type PFC cell. For application with low output voltage (e.g. ≤48 V), this high intermediate bus voltage increases components stresses on the DC/DC cell. With a simple step-down DC/DC cell (i.e. buck or buck-boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [9], [10]. Therefore, a high step-down transformer is usually employed even galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement [11]. Also, in some multi-stage power electronics system (e.g. in data centre, electrochemical and petrochemical industries, and subway applications [12]) the isolation has been done in the PFC stage, a second transformer in the DC/DC cell for the sake of isolation is considered as redundant. Hence, non-isolated AC/DC converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts [13]. In addition, the other drawbacks of the boost type PFC cell are that it cannot limit the input inrush current and provide output short circuit protection [14].

To tackle the above problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported [9], [10], [13], [15]–[18]. Although the recently reported IBoBuBo converter [13] is able to limit the bus voltage under 400 V, it cannot be applied to the low voltage application directly due to the boost PFC cell. On the other hand, the converters [9], [10], [15]–[18] employ different PFC cells to reduce the intermediate bus voltage. Among those converters, [9] and [15] use a transformer to achieve low output voltage either in PFC cell or DC/DC cell. Therefore, the leakage inductance is unavoidable.

In [10], [17], [18], the converters employ a buck-boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [18] and [10] process power at least twice resulting in low power efficiency. Moreover the reported converters, in [16], [17], consist of two active switches leading to more complicated gate control.

Apart from reducing the intermediate bus voltage, the converter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current-switching (ZCS) to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low frequency ripples on its output voltage. Besides, the duty cycle of the converter for high line input application is very narrow, i.e. ≤10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be given in the discussion section.

In this paper, an Intergrated Buck–Buck-Boost (IBuBuBo) converter with low output voltage is proposed. The converter utilises a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can
be achieved. Therefore, a transformer is not needed to obtain the low output voltage. To sum up, the converter is able to achieve:

1) Low intermediate bus and output voltages in the absence of transformer
2) Simple control structure with a single-switch
3) Positive output voltage
4) High conversion efficiency due to part of input power is processed once
5) Input surge current protection because of series connection of input source and switch.

The paper is organised as follows: operation principle of the proposed IBuBuBo converter is depicted in Section II and followed by design considerations with key equations in Section III. Experimental result and discussion of the converter are given in Section IV and V respectively. Finally, conclusion is stated in Section VI.

II. PROPOSED CIRCUIT AND ITS OPERATING PRINCIPLE

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell \((L_1, S_1, D_1, C_o, C_B)\) and a buck-boost DC/DC cell \((L_2, S_1, D_1, D_2, D_3, C_o, C_B)\) is illustrated in Fig. 1(a). Although \(L_2\) is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, \(L_2\) is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors \(L_1\) and \(L_2\) at the beginning of each switching cycle, \(t_0\). Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

Mode A \((v_{in}(\theta) \leq V_B + V_o)\): When the input voltage \(v_{in}(\theta)\) is smaller than the sum of intermediate bus voltage \(V_B\) and output voltage \(V_o\), the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage [20] owing to the reverse biased of the bridge rectifier. Only the buck-boost DC/DC cell sustains all the output power to the load. Therefore, two dead-angle zones present in a half line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is — Figs. 2(a)–2(b)–2(f). Fig. 3(a) shows its key current waveforms.

- Stage 1 (period \(d_1T_s\) in Fig. 3) [Fig. 2(a)]: When switch \(S_1\) is turned on, inductor \(L_2\) is charged linearly by the bus voltage \(V_B\) and diode \(D_2\) is conducting. Output capacitor \(C_o\) delivers power to the load.
- Stage 2 (period \(d_2T_s\) in Fig. 3) [Fig. 2(b)]: When switch \(S_1\) is switched off, diode \(D_1\) becomes forward biased and energy stored in \(L_2\) is released to \(C_o\) and the load.
- Stage 3 (period \(d_3T_s\) - \(d_4T_s\) in Fig. 3) [Fig. 2(f)]: The inductor current \(i_{L2}\) is totally discharged and only \(C_o\) sustains the load current.

Mode B \((v_{in}(\theta) > V_B + V_o)\): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into 4 stages and the corresponding sequence is — Figs. 2(c)–2(d)–2(e)–2(f). The key waveforms are shown in Fig. 3(b).

- Stage 1 (period \(d_1T_s\) in Fig. 3) [Fig. 2(c)]: When switch \(S_1\) is turned on, both inductors \(L_1\) and \(L_2\) are charged linearly by the input voltage minus the sum of the bus voltage and output voltage \((v_{in}(\theta) - V_B - V_o)\) and the bus voltage \(V_B\) respectively while diode \(D_2\) is conducting.
- Stage 2 (period \(d_2T_s\) in Fig. 3) [Fig. 2(d)]: When switch \(S_1\) is switched off, inductor current \(i_{L1}\) decreases linearly to charge \(C_B\) and \(C_o\) through diode \(D_1\) as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in \(L_2\) is released to \(C_o\) and supply current to the load through diode \(D_3\). This stage ends once inductor \(L_2\) is fully discharged.
- Stage 3 (period \(d_3T_s\) in Fig. 3) [Fig. 2(e)]: Inductor \(L_1\) continues to deliver current to \(C_o\) and the load until its current reaches zero.
- Stage 4 (period \(d_4T_s\) in Fig. 3) [Fig. 2(f)]: Only \(C_o\) delivers all the output power.

III. DESIGN CONSIDERATIONS

To simplify the circuit analysis, some assumptions are made as follows:

1) All components are ideal;
2) Line input source is pure sinusoidal, i.e. $v_{in}(\theta) = V_{pk}\sin(\theta)$ where $V_{pk}$ and $\theta$ are denoted as its peak voltage and phase angle respectively;

3) Both capacitors $C_B$ and $C_o$ are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;

4) The switching frequency $f_s$ is much higher than the line frequency such that the rectified line input voltage $|v_{in}(\theta)|$ is constant within a switching period.

A. Circuit Characteristics

According to Fig. 1(b), there is no input current drawn from the source in Mode A and the phase angles of the dead-time $\alpha$ and $\beta$ can be expressed as

$$\alpha = \arcsin\left(\frac{V_T}{V_{pk}}\right);$$

$$\beta = \pi - \alpha = \pi - \arcsin\left(\frac{V_T}{V_{pk}}\right).$$ (1)

where $V_T$ is the sum of $V_B$ and $V_o$. Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2\arcsin\left(\frac{V_T}{V_{pk}}\right).$$ (2)

From the key waveforms (Fig. 3), the peak currents of the two inductors are

$$i_{L1,pk} = \begin{cases} \frac{V_{pk}(\theta)-V_T}{L_1}d_1T_s & \alpha < \theta < \beta \\ 0 & \text{otherwise} \end{cases}$$ (3)

$$I_{L2,pk} = \frac{V_B}{L_2}d_1T_s$$ (4)

where $T_s (1/f_s)$ is a switching period of the converter. In (3) and (4), the dependency of $i_{L1,pk}$ on $\theta$ has been omitted for clarity. It is noted that $L_2$ does not contribute in (3) even through it is on the current return path of the PFC cell.

In addition, by considering volt-second balance of the $L_1$ and $L_2$ respectively, the important duty ratio relationships can
be expressed as follows:

\[ d_2 + d_3 = \begin{cases} \frac{v_{in}(\theta) - V_T}{L_1} d_1 & \alpha < \theta < \beta \\ 0 & \text{otherwise} \end{cases} \]

\[ d_2 = \frac{V_B}{V_o} d_1. \]  

By applying charge balance of \( C_B \) over a half line period, the bus voltage \( V_B \) can be determined. From Fig. 3, the average current of \( C_B \) over a switching and half line periods are expressed as follows:

\[
< i_{CB} >_{sw} = \frac{1}{2} \left( i_{L1,pk}(d_1 + d_2 + d_3) - I_{L2,pk} d_1 \right) = \frac{d_2^2 T_s}{2} \left[ \frac{v_{in}(\theta) - V_T v_{in}(\theta)}{L_1 V_T} - \frac{V_B}{L_2} \right]
\]

and

\[
< i_{CB} >_\pi = \frac{1}{\pi} \int_0^\pi < i_{CB} >_{sw} d\theta = \frac{d_2^2 T_s}{2\pi} \left[ V_{pk} \left( V_{pk} V_T \left( \frac{\gamma}{2} + \frac{A}{4} \right) - B \right) - \frac{\pi V_B}{L_2} \right]
\]

where the constants \( A \) and \( B \) are

\[
A = \sin(2\alpha) - \sin(2\beta); \quad B = \cos(\alpha) - \cos(\beta).
\]

Putting (8) to zero due to the steady state operation, this leads to

\[
V_B = \frac{M V_{pk}^2}{2\pi(V_B + V_o)} \times \left[ \pi - 2 \arcsin \left( \frac{V_B + V_o}{V_{pk}} \right) \right]
\]

\[
= \frac{2(V_B + V_o)}{\sqrt{(V_{pk} + V_B + V_o)(V_{pk} - V_B - V_o)}}
\]

where \( M \) is the inductance ratio \( L_2/L_1 \).

As observed from (11), the bus voltage \( V_B \) can be obtained easily by numerical method. It is noted that \( V_B \) is independent on the load but dependent on the inductance ratio \( M \). Fig. 4 depicts the relationship among \( V_B \), rms value of the line voltage and inductance ratio \( M \). It is noted that the bus voltage is kept below 150 V at high line input condition.

![Figure 4. Calculated intermediate bus voltage under different inductance ratios.](image)
the proposed circuit are

\[ < i_{in} >_{sw} = \frac{i_{L1, pk} d_1}{2} = \begin{cases} \frac{v_{in}(\theta) - V_T}{2\pi L_1} & \alpha < \theta < \beta \\ 0 & \text{otherwise} \end{cases} \]

and

\[ I_{in} = \frac{1}{\pi} \int_{\alpha}^{\beta} < i_{in} >_{sw} \, d\theta = \frac{d_1^2 T_s}{2\pi L_1} [v_{pk} B - \gamma V_T]. \]  

Using (12) and (13), the rms value of the input current, average input power and power factor are given by

\[ I_{in, rms} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\beta} < i_{in} >_{sw}^2 \, d\theta} = \frac{d_1^2 T_s}{2\sqrt{\pi} L_1} \sqrt{v_{pk}^2 \left( \frac{\gamma}{2} + \frac{A}{4} \right) - 2v_{pk} V_T B + \gamma V_T^2}; \]  

\[ P_{in} = \frac{1}{\pi} \int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} \, d\theta = \frac{d_1^2 T_s V_{pk}}{2\pi L_1} \left[ v_{pk} \left( \frac{\gamma}{2} + \frac{A}{4} \right) - V_T B \right]; \]  

\[ PF = \frac{1}{\pi} \int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} \, d\theta = \frac{d_1^2 T_s V_{pk}}{2\pi L_1} \frac{\sqrt{v_{pk}^2 \left( \frac{\gamma}{2} + \frac{A}{4} \right) - 2v_{pk} V_T B + \gamma V_T^2}}{V_{pk}^2 \left( \frac{\gamma}{2} + \frac{A}{4} \right)}; \]

B. Condition for DCM

To ensure both cells working in DCM mode throughout the AC line period, we must determine their critical inductance first. To allow \( L_1 \) working in DCM and from (5), we have the following inequalities:

\[ d_2 + d_1 \leq 1 - d_{1, PFC} \]  

and

\[ d_{1, PFC} \leq \left\{ \begin{array}{ll} \frac{V_T}{v_{in}(\theta)} & \alpha < \theta < \beta \\ 0 & \text{otherwise} \end{array} \right. \]

where \( d_{1, PFC} \) is the maximum \( d_1 \) of the PFC cell.

For the buck-boost DC/DC cell working in DCM mode, the following inequality must be held:

\[ d_2 \leq 1 - d_{1, DC/DC}. \]

From (6) and (19), the maximum \( d_1 \) of the DC/DC cell is

\[ d_{1, DC/DC} \leq \frac{V_o}{V_o + V_B} = \frac{V_o}{V_T}. \]

Due to sharing switch in both cells of the converter, the maximum duty cycle \( d_{1, max} \) of the proposed converter is

\[ d_{1, max} = \begin{cases} \min(d_{1, PFC}, d_{1, DC/DC}) & \alpha < \theta < \beta \\ d_{1, DC/DC} & \text{otherwise} \end{cases} \]

By applying input-output power balance of the PFC cell and substituting (21) into (15), the critical inductance \( L_{1, crit} \) is given by

\[ L_{1, crit} = \frac{R_{L, min} T_s V_{pk} V_T}{2\pi V_o^2} \left[ v_{pk} \left( \frac{\gamma}{2} + \frac{\sin(2\alpha) - \sin(2\beta)}{4} \right) + V_T (\cos(\beta) - \cos(\alpha)) \right] d_{1, max}^2. \]

where \( R_{L, min} \) is denoted as the minimum load resistance of the converter.

For the DC/DC cell sustaining all the power to the load under DCM operation in Mode A, the critical inductance \( L_{2, crit} \) is the smallest. Under the input–output power balance of the DC/DC cell, the critical inductance \( L_{2, crit} \) can be determined. The input power of the DC/DC cell in Mode A is given by

\[ P_{in, DC/DC} = \frac{V_B}{\pi} \int_0^{< i_{DC/DC} >_{sw}} d\theta = \frac{V_B^2 T_s}{2L_2} d_1^2 \]

where \( < i_{DC/DC} >_{sw} \) is the instantaneous input current of DC/DC cell.

Hence, by substituting (21) into (23), the critical inductance \( L_{2, crit} \) is given by

\[ L_{2, crit} = \frac{R_{L, min} V_B^2 T_s}{2V_o^2} d_{1, max}^2. \]
C. Components Stresses

Before embarking on calculating stresses on the devices, there are two characteristics of the circuit to be clarified. Interestingly, the current passing through the diode $D_2$ is the difference of current between $i_{L2}$ and $i_{L1}$ at the time interval $d_1 T_s$. Both inductor currents flows into the diode at the interval but in opposite direction. In addition, unlike the boost type single-stage AC/DC converter, the current of the switch $S_1$ is $i_{L2}$, but not the superposition current of both inductors. Thus, the simultaneous currents of the diode $D_2$ and switch $S_1$ at interval $d_1 T_s$ are

\begin{align}
  i_{D_2} &= i_{L2} - i_{L1}; \quad (25) \\
  i_{S_1} &= i_{L2}. \quad (26)
\end{align}

The rms current stresses on the diodes and switch are determined by averaging their rms current in a switching cycle over a half line period. The rms current stress on the diode $D_1$ over a switching cycle is

\[
I_{D_1,rms} = \frac{T_s}{L_1} \sqrt{\frac{1}{3} \left( v_{in}(\theta) - 2 V_T \right)^2}.
\]

Then, by taking the average of (27) over a half line period, its rms current stress is obtained as (28), shown at the top of the next page, where $C = \cos(3\alpha) - \cos(3\beta)$.

Similarly, the current stresses on the other semiconductor devices can be calculated easily as

\begin{align}
  I_{D_2,hf,rms} &= \frac{T_s}{L_2} \sqrt{\frac{d_1^3}{3\pi} \left[ 2\alpha V_B^2 + E \right]}; \quad (29) \\
  I_{D_3,hf,rms} &= \frac{V_B T_s}{L_2} \sqrt{\frac{d_1^3 (V_B - V_0)^3}{3}}; \quad (30) \\
  I_{S_1,hf,rms} &= \frac{V_B T_s}{L_2} \sqrt{\frac{d_1^3}{3}}; \quad (31)
\end{align}

where

\[
E = \frac{1}{L_1^2} \left[ \gamma (V_B L_T + L_2 V_o)^2 - 2L_2 V_{pk} B (V_B (L_1 + L_2) + L_2 V_o) + \frac{L_2^2 V_{pk}^2}{2} \left( \gamma + \frac{A}{2} \right) \right].
\]

In addition, the voltage stresses on the semiconductor devices are stated in table I.

<table>
<thead>
<tr>
<th>Semiconductor devices</th>
<th>Peak Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode $D_1$</td>
<td>$V_{pk}$</td>
</tr>
<tr>
<td>Diode $D_2$</td>
<td>$V_{pk}$</td>
</tr>
<tr>
<td>Diode $D_3$</td>
<td>$V_T$</td>
</tr>
<tr>
<td>Switch $S_1$</td>
<td>$V_{pk} + V_T$</td>
</tr>
</tbody>
</table>

D. Capacitors Optimization

To determine the size of the intermediate bus capacitor $C_B$, we can consider the hold-up time ($t_{hold_up}$) of the circuit. The bus capacitor $C_B$ will sustain all the output power within $t_{hold_up}$ when the AC input source is removed. In normal practice, the hold-up time is one of the AC line cycle. In addition, the maximum capacitance of $C_B$ to meet this hold-up time requirement is determined under the low line and full output load conditions. Thus, the size of $C_B$ is expressed as follows:

\[
C_B = \frac{2 P_o t_{hold_up}}{V_B @ 90 V_{rms}^2}. \quad (32)
\]

Apart from the size of $C_B$, it is noted that the line frequency ripple on the output capacitor $C_o$ is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

E. Distribution of Direct Power Transfer

The interaction of power processing between both PFC and DC/DC cells under low and high line conditions is described as

\[
p_o(\theta) = p_{o,PFC}(\theta) + p_{o,DC/DC}(\theta) \quad (33)
\]

where $p_{o,total}(\theta)$, $p_{o,PFC}(\theta)$ and $p_{o,DC/DC}(\theta)$ are denoted as instantaneous output power of the converter, output power of PFC cell and output power of DC/DC cell respectively.

Both instantaneous output powers of PFC and DC/DC cells can be calculated as

\[
p_{o,PFC}(\theta) = V_o (i_{L1}(\theta))_{sw} = \begin{cases} 
(d_1(\theta))^2 V_T \left[ v_{in}(\theta) - V_T \right] & \alpha < \theta < \beta \\
0 & \text{otherwise}
\end{cases} \quad (34)
\]

\[
p_{o,DC/DC}(\theta) = \begin{cases} 
V_T^2 T_s & \text{otherwise}
\end{cases} \quad (35)
\]

where $p_{in,DC/DC}(\theta)$ and $d_1(\theta)$ are defined as the instantaneous value of input power of the DC/DC cell and duty cycle $d_1$.

From (34) and (35), it can be seen that $d_1(\theta)$ plays a crucial role in this analysis. $d_1(\theta)$ can be obtained easily once the average output current of the converter is determined. By considering the average currents of $i_{L1}$ and $i_{L3}$ over a switching cycle, the average output current of the converter is given by

\[
I_o = \begin{cases} 
(i_{L1}(\theta))_{sw} + (i_{L3}(\theta))_{sw} & \alpha < \theta < \beta \\
(i_{L3}(\theta))_{sw} & \text{otherwise}
\end{cases} \quad (36)
\]

Hence, $d_1(\theta)$ in a half line period is expressed as

\[
d_1(\theta) = \begin{cases} 
\sqrt{\frac{2 P_o}{V_{pk} T_s \left[ v_{in}(\theta) - V_T \right]}} & \alpha < \theta < \beta \\
\sqrt{\frac{2 P_o V_T^2}{V_{pk} T_s}} & \text{otherwise}
\end{cases} \quad (37)
\]

By substituting (37) into (34) and (35), the simultaneous output power of the converter and power distribution of the PFC and DC/DC cells are plotted as in Fig. 6. The traces of
\[ I_{D1,hf,rms} = \frac{T_s}{3V_T L_1} \sqrt{\frac{d_t^3}{\pi}} \left[ -\gamma V_T (8V_T^2 + 3V_T^2) + 3V_T B\left(\frac{V_T^2}{4} + 4V_T^2\right) - \frac{3V_T V_T^2 A}{2} - \frac{V_T^3 C}{12} \right] \] (28)

Figure 6. Calculated power processing by PFC cell (red trace) and DC/DC cell (blue trace). Condition: \( P_o = 100 \text{ W} \) (green trace), \( V_o = 19 \text{ V} \) and \( M = 0.4 \).

single and double power processing represent the power processed by PFC cell \( (p_{D, PFC}(\theta)) \) and DC/DC cell \( (p_{D, DC/DC(\theta)}) \) respectively. Besides, the green dash trace is the output power \( (p_{D, total}(\theta)) \) of the converter. It is noted that the power handled by both cells is changed oppositely to maintain the load power under different input voltages. At low line condition, there is more input power coupled to the output directly. In contrast, more power is delivered to the output by the DC/DC cell at high line condition. More discussion of the direct power transfer will be given in Section V.

IV. EXPERIMENTAL RESULTS

The performance of the proposed circuit is verified by the prototype. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power factor (> 96%), the inductance ratio has to be optimized according to Figs. 4 and 5. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used. In addition, the inductance ratio will affect the efficiency of the converter. More detail will be given in Discussion section. Taking the performance of the converter on bus voltage, power factor and efficiency into account, the inductance ratio around \( M = 0.4 \) is selected. Table II depicts all the components used in the circuit, and its specification is stated as follows:

1) Output power: 100 W;
2) Output voltage: 19 Vdc;
3) Power factor: > 96%;
4) Intermediate bus voltage: < 150V;
5) Line-input voltage: 90 ~ 270 Vrms/50 Hz;
6) Switching frequency \( (f_s) \): 20 kHz.

![Diagram](image)

Fig. 7 shows the waveforms of the line input voltage along with its current under full load condition at 90 Vrms and 270 Vrms respectively. The measured current harmonics met the IEC61000-3-2 class D standard as shown in Fig. 8. In addition, the measured output and bus voltages under both low and high line conditions are shown as in Fig. 9. It can be seen that the bus voltage was kept at 123 V and well below 150 V at high line condition. Fig. 10 illustrates the conversion efficiency of the proposed converter under different line input and output power conditions. The maximum efficiency of the circuit is around 89% at low line application. Furthermore, Fig. 11 shows the predicted intermediate bus voltage is in good agreement with the measured value.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>R. Controller</td>
<td>ILS94</td>
</tr>
<tr>
<td>Input filter inductor ( L_1 )</td>
<td>2 mH</td>
</tr>
<tr>
<td>Input filter capacitor ( C_f )</td>
<td>4 ( \mu )F</td>
</tr>
<tr>
<td>Inductor ( L_1 )</td>
<td>106 ( \mu )H</td>
</tr>
<tr>
<td>Inductor ( L_2 )</td>
<td>46 ( \mu )H</td>
</tr>
<tr>
<td>Inductance Ratio ( (M = L_2/L_1) )</td>
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</tr>
<tr>
<td>MOSFET ( S_1 )</td>
<td>SPW47N60CFD</td>
</tr>
<tr>
<td>( D_1 )</td>
<td>MUR3040PT</td>
</tr>
<tr>
<td>( D_2 )</td>
<td>MUR3040PT</td>
</tr>
<tr>
<td>( L_2 )</td>
<td>5 mF</td>
</tr>
<tr>
<td>( C_{3} )</td>
<td>5 mF</td>
</tr>
</tbody>
</table>

Table II CIRCUIT COMPONENTS.
(a) Line input voltage (Upper Trace - 100V/div) along with its input current (Bottom Trace - 2 A/div)

(b) Line input voltage (Upper Trace - 250V/div) and input current (Bottom Trace - 1 A/div)

Figure 7. Measured input characteristic of the converter at (a) 90 Vrms and (b) 270 Vrms under 100 W condition.

Figure 8. Comparison of IEC61000-3-2 Class D standard with measured input current harmonics at 270 Vrms.

conversion around ten times at high line condition, from $V_B = 123$ V down to $V_o = 19$ V. As a result, it further impairs the the efficiency of the converter at high line operation. On the other hand, from (2), decrease of $V_B$ extends the conduction angle of the converter leading to higher power factor. However, lower $V_B$ requires decrease of inductance ratio resulting in higher peak inductor currents and causing higher conduction loss. Thus, tradeoff has to be made for selecting the inductance ratio among the peak current of both inductors, bus voltage and power factor. Nevertheless, the converter is capable to be used at high line condition with the full load efficiency around

84% at 240 Vrms.

To continue the comparison from the Introduction section, Table III shows the performances of recent topologies and the proposed converter in more detail. In order to achieve low output voltage and low intermediate bus voltage with high efficiency for universal line operation, the topologies employ different approaches. Furthermore, every converter has their best performance when working at particular input and output conditions. Although the input and output conditions for the converters in the table are not the same, we have two criteria

Figure 9. Measured output voltage (Upper Trace -10V/div) and intermediate bus voltage (Bottom Trace - 40V/div) at (a) 90 Vrms and (b) 270 Vrms under full load condition.

Figure 10. Measured circuit efficiency under load variation.
to compare their performances. First, for a given power level, the lower output voltage of the converter, the lower efficiency it gets due to more current flowing in the circuit. Second, for PWM converters, the fewer semiconductor devices used in the converter, the less conduction and switching loss of the converter will be. However, the operational parameters, selection of switching frequency and semiconductor, will also impact on the circuit efficiency. Therefore it is hard to have a fair efficiency comparison and hence circuit efficiencies shown are just for information purpose. Nevertheless, apart from the efficiency, the performances on reducing the bus voltage, the step-down ratio and circuit complexity are less dependent to the input and output conditions, and operational parameters but the topology itself and the inductance ratio. From the table and excluding all the isolated converters, it can be seen that the proposed converter is able to achieve the lowest bus voltage at high line condition with low output voltage and probably higher efficiency among all transformerless topologies and its structure is simpler. In addition, comparing with [10], [18] at low line condition, the proposed converter is also able to achieve the lowest bus voltage at around 33.5 V with positive output voltage and probably higher efficiency. Thus, the proposed converter has better performance for lower output voltage operation.

VI. CONCLUSION

The proposed Integrated Buck–Buck-Boost (IBuBuBo) single-stage AC/DC converter has been experimentally verified, and the results have shown good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below 150 V at all input and output conditions and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short circuit protection. Thanks to the direct power transfer path in the proposed converter, it is able to achieve high efficiency around 89%.

REFERENCES


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