Implementation of an Efficient Transformerless Single-Stage Single-Switch AC/DC Converter

Abstract—A transformerless single-stage single-switch AC/DC converter is presented in this paper. The converter allows a portion of the input power to be processed once only, resulting in enhanced conversion efficiency. Additionally, due to the absence of transformer, the size and manufacturing cost of the converter can be reduced. The intermediate bus voltage is well kept below 400 V while maintaining high power factor even at light load and high line input conditions. Extended experimental results on a 100-W hardware prototype for universal input voltage range (90 Vrms-270 Vrms) are given to confirm the theoretical analysis and performance of the proposed converter.

Index Terms—AC/DC converter, power-factor-correction (PFC), single-stage (SS) and universal line input

I. INTRODUCTION

Due to the stringent current harmonics regulations [1]-[2], which are imposed on single phase AC/DC power supplies, inclusion of a power factor correction (PFC) circuit in the power supply design becomes mandatory. Conventional AC/DC power supply design uses a cascade connection of a PFC circuit followed by a DC/DC converter. Many single-stage (SS) AC/DC converters have been reported. The SS AC/DC converter reduces cost, size and complexity in the control loop by combining PFC cell with a post DC/DC cell and using one common set of switching control signal. It is a very attractive solution in low power applications where the manufacturing cost and size of converter are the major issues. The underlying principle for the SS AC/DC conversion is to force the PFC cell inductor operating in discontinuous conduction mode (DCM) for achieving high power factor automatically without any control loop whereas the well and tight output regulation is done by post DC/DC stage (SS) AC/DC converters have been reported. The SS AC/DC converter allows a portion of ac input power directly coupled to the output, was reported. In other words, the input power was processed twice resulting in low efficiency.

In general, for some output voltage levels, most single stage converters which operate in DCM cannot be used in wide universal line input range because of narrow duty cycle which impairs converter efficiency or may limit the input voltage range for getting better performance [18], [20]-[23]. The instantaneous duty cycle is determined by the DC/DC cell as long as the inductor of the PFC cell can be operated in DCM in the entire operation. In other words, this inductance restricts the maximum duty cycle of the converter itself. By adjusting the inductance ratio in the two cells, the bus capacitor voltage \( V_B \), which is the input voltage of DC/DC cell, can be determined. Therefore, the simultaneously duty cycle is bounded by the maximum duty cycle. In normal practice, the chosen inductor value of the PFC cell is smaller than the calculated critical inductance at minimum line input voltage. Compared with the value calculated at high line input, it can be four times smaller. Therefore, this chosen inductance is too small at high line condition leading to very high RMS current and narrow duty cycle (usually less than 0.1). The reported converters and proposed converter would also encounter the same problem of extremely low duty cycle at high line condition for universal line operation for other applications and different output voltage levels. To mitigate extremely narrow duty cycle (<10%) operation at high line application, higher switching frequency is used in this paper. Unlike BCM operation with variable switching frequencies,

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only two fixed frequencies are used in the proposed circuit to avoid wide frequency span. The higher switching frequency is only used in the condition of extremely narrow duty cycle at high line input for universal line applications. Otherwise, it may impair the converter efficiency due to significant of switching loss.

It should be mentioned that the proposed converter is not suitable for extremely step-down conversion due to absence of transformer but can be used in DC bus distribution system in [24] and in the industry directly without galvanic isolation requirement. Fig. 1 shows modified version of the converter in [25] and [26]. The proposed circuit has similar characteristics to that of [25] and [26]. However, compared with the reported circuit in [25], which aims for pre-regulation with power factor correction feature, a blocking diode $D_1$ is added in series with the inductor $L_1$ in the proposed converter to avoid energy from the bus capacitor transferring back to the input resulting in line current distortion [26]. Although [26] mainly discusses the soft-switching cell in a modified SEPIC converter, in this paper, its fundamental characteristic without soft-switching cell will be discussed in order to have a fair comparison. In addition, the reported circuit in [25] and the proposed circuit can solve the high start-up inrush current problem, which can damage the inductor ($L_1$) and switching diodes ($D_1$ and $D_2$) in Fig. 1, by a bypass diode like using in a boost converter whereas it cannot be put in the reported circuit [26]. The three converters have a characteristic that the output voltage can be lower than the input voltage. Therefore, the bypass diode cannot be utilized in [26]. To solve this problem, [25] and the proposed circuit place the bus capacitor $C_B$ in the current return path and now the line peak voltage charges both $C_o$ and $C_B$ in series instead. The total voltage of two capacitors must be greater than the line peak voltage due to the characteristic of boost PFC cell. However, both [25] and [26] did not report detailed circuit analysis and design consideration. Also, while the two converters in [25] and [26] work in boundary conduction mode, the analysis and design of the proposed converter is based on DCM operation.

This paper intends to verify performance of changing switching frequency for operating in universal line input, and to give extended analysis and experimental results of [27] in terms of circuit design consideration, performance analysis and controller design. Moreover, using higher switching frequency and working in DCM achieve smaller size of inductors and result in higher power density with compatible efficiency. Section II gives a review of circuit operation briefly. The discussion of circuit considerations will be given and followed by experimental results in section III and IV respectively. Finally, conclusion is stated in V.

II. REVIEW OF CIRCUIT OPERATION

The schematic of the proposed converter, which consists of a boost PFC cell ($L_1$, $S_1$, $D_1$, $D_2$, $C_o$ and $C_B$) and a buck-boost DC/DC cell ($L_2$, $S_1$, $D_2$, $D_3$, $C_o$ and $C_B$) is illustrated in Fig. 1. Both cells are operated in DCM. The circuit operations within a switching period can be divided into 4 stages and its corresponding current waveforms are shown in Fig. 2. 1) Stage 1 (interval $d_1$): Prior to this interval, all the currents in the inductors $L_1$ and $L_2$ are at zero level owing to DCM operation of the two cells. When switch $S_1$ is turned on at $t_0$, both $L_1$ and $L_2$ are charged linearly by the line input voltage and bus capacitor voltage $V_B$ respectively. Meanwhile, diode $D_2$ is reverse biased and clamped to $V_T$ ($V_B + V_o$) so energy stored in $C_o$ sustains the load current. This stage is ended until switch $S_1$ is turned off.

2) Stage 2 (interval $d_2$): When $S_1$ is turned off, diode $D_2$ becomes forward biased so current $i_{L1}$ decreases linearly to charge up $C_o$ and $C_B$ as well as transferring part of power to the load. At the same time, $i_{L2}$ discharges through diode $D_2$ and $D_3$ to charge $C_o$ together to provide current to the load. The drain-to-source voltage of $S_1$ is clamped to $V_T$. This stage completes when the inductor current in $L_1$ is totally discharged. 3) Stage 3 (interval $d_3$): During this mode, $i_{L2}$ still remains discharging and delivering current to $C_o$ and the load through diode $D_2$ and $D_3$ until it reaches zero. Note that there exists a situation where the current $i_{L1}$ may reach ground level after current $i_{L2}$ and $d_3$ goes negative. Therefore, this will not affect the analysis because this situation will be revealed in $d_3$. More details will be given in Section III. 4) Stage 4 (interval $d_4$): Both currents in $i_{L1}$ and $i_{L2}$ are totally discharged and only $C_o$ sustains the load current.

Detailed circuit analysis and equations have been presented in [27].

III. CIRCUIT CONSIDERATIONS

A. Switching Frequency Circuit

From (15) in [27], it is restated as (1) and the detailed derivation is given in the appendix. It can be seen that the averaged duty cycle over the half line period depends on the inductance of the PFC cell, switching frequency, input
According to (1), the input and output conditions and inductance value are normally fixed by its design and specification, so the only way to extend the duty cycle at high line operation is to increase the switching frequency.

\[
d_1 = \sqrt{\frac{2\pi L_{1} f_s P_o V_o}{V_{in,pk}^2 (P_o R_L + V_B V_o) \int_0^\pi \frac{\sin^2 \theta}{V_T - V_{in,pk} \sin \theta} d\theta}}
\]  

(1)

To alleviate the aforementioned problems caused by the narrow duty cycle at high line condition, two switching frequencies are selected: 100 kHz for 90 Vrms to 150 Vrms, and 200 kHz for 150 Vrms to 270 Vrms. The reason for selecting 150 Vrms as a turning point is that this voltage is not a common voltage level for commercial and industrial applications even in low and high line applications. Even if 150 Vrms is a critical voltage, other voltage can be set as a turning point. Using the voltage-mode PWM controller TL494 for an example, switching frequency block in Fig. 3 shows the frequency selection circuit. For clarity, only the part which selects the switching frequency is illustrated. The rest of the components of the controller can be determined according to its application note and datasheet. 

C. Condition for DCM

The condition for the inductance required for \( L_1 \) to be in DCM has been found in [27] which is re-stated as (2).

\[
L_1 \leq \left(1 - \frac{V_{in,pk,min}}{V_T}\right)^2 \frac{R_L \min V_T V_{in,pk,min}^2}{2\pi V_o^2 f_s,\min} \times \int_0^\pi \frac{\sin^2 \theta}{V_T - V_{in,pk} \sin \theta} d\theta
\]  

(2)

Similarly, the critical inductance for \( L_2 \) operating in DCM can be obtained by applying input-output power balance principle. The input and output voltages in the DC/DC cell can be considered as constant due to sufficiently large capacitances in the bus capacitor and output capacitor. Therefore,

\[
P_{in,DC/DC} = V_B \langle i_{DC/DC} \rangle_{su} = (1 - n)P_o
\]  

(3)
The averaged input current for the DC/DC cell is

\[ \langle i_{DC/DC} \rangle_{sw} = \frac{V_B}{2L_2f_s} d_1^2 \]  

(4)

Putting (3) into (4), inductance \( L_2 \) can be found

\[ L_2 = \frac{V_BR_LV_T}{2V_o^2f_s} d_1^2 \]  

(5)

By considering the volt-second balance on \( L_2 \) and its condition working in DCM, the following inequalities are obtained.

\[ d_2 + d_3 = \frac{V_B}{V_o} d_1 \]  

(6)

\[ d_2 + d_3 \leq 1 - d_1 \]  

(7)

\[ d_1 \leq \frac{V_o}{V_T} \]  

(8)

By putting (8) into (5), the condition for inductor \( L_2 \) operating in DCM is

\[ L_2 \leq \frac{V_BR_{L,min}}{2V_Tf_{s,min}} \]  

(9)

In order to curb the voltage on the bus capacitor well below 400 V and maintain the power factor around 95% at 270 Vrms, the inductance ratio around 0.7 is chosen from Figs. 4 and 5 in [27]. Based on (2), (9) and the optimized inductance ratio (0.7), \( L_1 \) and \( L_2 \) can be determined.

D. Duty Cycle and Devices Stress

To begin with calculating components current stress, the relationship among instantaneous values of \( d_1, d_2 \) and \( d_3 \) must be found. Putting (1) in [27], stated as (10), into (6), this yields (11).

\[ d_1 = \frac{V_T - |v_{in}(\theta)|}{|v_{in}(\theta)|} d_2 \]  

(10)

\[ d_3 = \left( \frac{V_B}{V_o} - \frac{|v_{in}(\theta)|}{V_T - |v_{in}(\theta)|} \right) d_1 \]  

(11)

where \( v_{in}(\theta) \) is \( v_{in, pk} \sin \theta \).

It should be noticed that \( d_3 \) may go to negative for the situation where \( V_B/V_o \) is smaller than \( |v_{in}(\theta)|/(V_T - |v_{in}(\theta)|) \). This means the discharging current of \( L_2 \) reaches zero prior to \( i_{L1} \). However, it does not affect the above analysis and the analysis in [27] as this situation is automatically revealed in \( d_3 \).

The average output current is found by averaging the diode current \( i_{d2} \) over a switching cycle.

\[ I_o = \langle i_{d2}(\theta) \rangle_{sw} = \frac{1}{2f_s} \left( \frac{V_T - |v_{in}(\theta)|}{L_1} d_2^2 + \frac{V_o}{L_2} (d_2 + d_3)^2 \right) \]

\[ = d_1^2 \left( \frac{|v_{in}(\theta)|^2}{L_1(V_T - |v_{in}(\theta)|)} + \frac{V_o^2}{V_oL_2} \right) \]

(12)

Therefore, the simultaneous value \( d_1 \) is

\[ d_1(\theta) = \sqrt{\frac{2P_0f_sL_1L_2(V_T - |v_{in}(\theta)|)}{L_oV_o|v_{in}(\theta)|^2 + B_2L_1(V_T - |v_{in}(\theta)|)^2}} \]

(13)

Based on (13) and the circuit parameters in Table I, the value of \( d_1(\theta) \) over a half-line period at 270 Vrms can be plotted as in Fig. 4. It can be seen that \( d_1(\theta) \) is below 0.1 throughout the operation working at 100 kHz while the duty cycle is extended to over 0.1 when doubling the switching frequency.

The rms current stress on the switch is determined by averaging its rms current in one switching cycle over a half line period. The switch rms current in one switching cycle is

\[ I_{s1,sw\_rms}(\theta) = \left( \frac{V_B}{L_2} + \frac{|v_{in}(\theta)|}{L_1} \right) \sqrt{\frac{d_1^3}{3f_s^2}} \]  

(14)

Averaging (14), rms switch current over a half line period is

\[ I_{s1,hf\_rms} = \frac{1}{f_s} \left( \frac{\pi V_B}{L_2} + \frac{2V_{in, pk}}{L_1} \right) \sqrt{\frac{d_1^3}{3}} \]  

(15)

Similarly, the rms currents of diodes and inductors are

\[ I_{D1, hf\_rms} = I_{L1, hf\_rms} = \frac{1}{\pi f_s L_1} \left( \int_0^\pi |v_{in}(\theta)| \sqrt{1 + \frac{|v_{in}(\theta)|}{V_T - |v_{in}(\theta)|}} d\theta \right) \]

(16)

\[ I_{D2, hf\_rms} = I_{L2, hf\_rms} = \frac{V_B}{L_2 f_s} \left( \frac{d_1^3}{3} + 1 + \frac{V_B}{V_o} \right) \]

(17)

\[ I_{D3, hf\_rms} = \int_0^\pi \sqrt{\frac{|v_{in}(\theta)|^3}{L_1^2(V_T - |v_{in}(\theta)|)}} + \frac{V_B^3}{L_2^2V_o} d\theta \times \frac{1}{\pi f_s} \sqrt{\frac{d_1^3}{3}} \]  

(18)

E. Low Frequency Small-Signal Modeling

Using state space averaging, the low frequency small-signal model of the proposed circuit can be derived. There are four energy storage elements in the converter \( L_1, L_2, C_o \) and \( C_B \) but only the voltages on \( C_o \) and \( C_B \) are considered as state variables due to no net stored inductor energy in a switching period. For brevity, the notation \( \ddot{x}(\theta) \) denotes the moving average \( \langle x(\theta) \rangle_{sw} \) over a switching period.

The averaged current of the bus capacitor in a switching period, (5) in [27] is rewritten as (19), and its averaged value
respectively.

\[ \bar{i}_B(\theta) = \frac{d_1^2}{2f_s\pi L_1} \int_0^\pi \frac{(\bar{v}_{in,pk}\sin\theta)^2}{\bar{v}_B + \bar{v}_{co} - \bar{v}_{in,pk}\sin\theta} \, d\theta - \frac{\bar{v}_B}{L_2} \]  

(19)

\[ \left( \bar{i}_B(\theta) \right)_\pi = \frac{d_1^2}{2f_s\pi L_1} \int_0^\pi \frac{(\bar{v}_{in,pk}\sin\theta)^2}{\bar{v}_B + \bar{v}_{co} - \bar{v}_{in,pk}\sin\theta} \, d\theta - \frac{\bar{v}_B}{L_2} = g(\bar{v}_B, \bar{v}_{co}, \bar{v}_{in,pk}, d_1) \]  

(20)

From (10), (11) and Fig. 2, the averaged output capacitor current over a switching and half line cycle are as follows:

\[ \bar{i}_{co}(\theta) = -\bar{v}_{co} + \frac{d_1^2}{2f_s L_1} \left( \frac{(\bar{v}_{in,pk}\sin\theta)^2}{\bar{v}_B + \bar{v}_{co} - \bar{v}_{in,pk}\sin\theta} + \frac{\bar{v}_B}{\bar{v}_o L_2} \right) \]  

(21)

\[ \left( \bar{i}_{co}(\theta) \right)_\pi = -\bar{v}_{co} + \frac{d_1^2}{2\pi f_s L_1} \left( \frac{(\bar{v}_{in,pk}\sin\theta)^2}{\bar{v}_B + \bar{v}_{co} - \bar{v}_{in,pk}\sin\theta} \right) + \frac{\bar{v}_B}{\bar{v}_o L_2} \right) \]  

\[ = h(\bar{v}_B, \bar{v}_{co}, \bar{v}_{in,pk}, d_1) \]  

(22)

A linearized ac small signal model equation can be obtained by perturbing (20) and (22) with \( v_{co} = V_{co} + \bar{v}_{co} \), \( v_B = V_B + \bar{v}_B, \bar{v}_{in,pk} = V_{in,pk} + \bar{v}_{in,pk} \) and \( d_1 = D_1 + \bar{d}_1 \) where \( V_{co} \gg \bar{v}_{co}, V_B \gg \bar{v}_B, V_{in,pk} \gg \bar{v}_{in,pk} \) and \( D_1 \gg \bar{d}_1 \).

By neglecting high-order non-linear terms and the products of the small-signal terms, the small signal equation can be written as in matrix form (23) with the output equation \( \bar{v}_{co} = \bar{v}_o \).

Taking Laplace transform of (23), this leads to line to output and control to output transfer functions in (24) and (25) respectively.

\[
\begin{bmatrix}
\bar{v}_B \\
\bar{v}_{co}
\end{bmatrix}
= \begin{bmatrix}
\frac{b_{11}}{C_{B}} & \frac{b_{12}}{C_{B}} \\
\frac{b_{41}}{C_{o}} & \frac{b_{42}}{C_{o}}
\end{bmatrix}
\begin{bmatrix}
\bar{v}_B \\
\bar{v}_{co}
\end{bmatrix}
+ \begin{bmatrix}
b_{11} \bar{v}_{in,pk} \\
b_{41} \bar{v}_{in,pk}
\end{bmatrix}
\]

(23)

\[
H_c(s) = \frac{\bar{v}_o(s)}{\bar{v}_{in,pk}(s)} \Big|_{\bar{v}_{in,pk} = 0} = \frac{b_{11}s + a_{11}b_{11} - a_{12}b_{21}}{s^2 + \frac{a_{11}}{C_{B}}(s^{2} + \frac{a_{41}}{C_{B}}) - \frac{a_{12}a_{22}}{C_{B}C_{o}}} \]

(24)

\[
H_d(s) = \frac{\bar{v}_d(s)}{\bar{d}_1(s)} \Big|_{\bar{v}_{in,pk} = 0} = \frac{b_{21}s + a_{21}b_{21} - a_{22}b_{22}}{s^2 + \frac{a_{41}}{C_{B}}(s^{2} + \frac{a_{41}}{C_{B}}) - \frac{a_{22}a_{22}}{C_{B}C_{o}}} \]

(25)

where

\[
\begin{align*}
a_{11} &= \left. \frac{\partial \bar{v}}{\partial \bar{v}_{co}} \right|_p, & a_{12} &= \left. \frac{\partial \bar{v}}{\partial \bar{v}_{co}} \right|_p, & a_{21} &= \left. \frac{\partial \bar{v}}{\partial \bar{v}_{co}} \right|_p, & a_{22} &= \left. \frac{\partial \bar{v}}{\partial \bar{v}_{co}} \right|_p, \\
b_{11} &= \left. \frac{\partial \bar{v}_{in,pk}}{\partial \bar{v}_{in,pk}} \right|_p, & b_{12} &= \left. \frac{\partial \bar{v}_{in,pk}}{\partial \bar{v}_{in,pk}} \right|_p, & b_{21} &= \left. \frac{\partial \bar{v}_{in,pk}}{\partial \bar{v}_{in,pk}} \right|_p, & b_{22} &= \left. \frac{\partial \bar{v}_{in,pk}}{\partial \bar{v}_{in,pk}} \right|_p.
\end{align*}
\]

(26)

The transfer functions cannot be expressed in analytical form but can be solved in numerical method easily.

### IV. EXPERIMENTAL RESULT

The performance of the proposed circuit is verified by the prototype. Table I depicted all the components used in the circuit and its specification is stated as follows:

- Output Power: 100 W
- Output Voltage: 100 Vdc
- Line input Voltage: 90 ~ 270 Vrms / 50 Hz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency (f_s)</td>
<td>100 kHz (90 Vrms ~ 150 Vrms)</td>
</tr>
<tr>
<td>200 kHz (150 Vrms ~ 270 Vrms)</td>
<td></td>
</tr>
<tr>
<td>IC Controller</td>
<td>TL494</td>
</tr>
<tr>
<td>IC for frequency selection</td>
<td>LM393</td>
</tr>
<tr>
<td>Input filter inductor L_f</td>
<td>1.92 mH with RESR = 850 mΩ</td>
</tr>
<tr>
<td>Input filter capacitor C_f</td>
<td>1 μF</td>
</tr>
<tr>
<td>Inductor L_1</td>
<td>88.4 μH with RESR = 187 mΩ</td>
</tr>
<tr>
<td>Inductor L_2</td>
<td>68.6 μH with RESR = 128 mΩ</td>
</tr>
<tr>
<td>Inductance Ratio (M = L_2/L_1)</td>
<td>0.776</td>
</tr>
<tr>
<td>MOSFET S_1</td>
<td>IRFP250PBF</td>
</tr>
<tr>
<td>D_1</td>
<td>MUR860 x2</td>
</tr>
<tr>
<td>D_2</td>
<td>MUR860</td>
</tr>
<tr>
<td>D_3</td>
<td>MBR820200</td>
</tr>
<tr>
<td>C_B</td>
<td>470 uF with RESR = 240 mΩ</td>
</tr>
<tr>
<td>C_o</td>
<td>470 μF X 2 with RESR = 240 mΩ</td>
</tr>
</tbody>
</table>

per each

According to (1) and the above-mentioned specification, the averaged duty cycle at 270 Vrms line input at full load condition can be improved from 8.5% in 100 kHz to 12% in 200 kHz. Based on the circuit parameters, we can get the matrix coefficients.

\[
a_{11} = -3.088 \times 10^{-3}, & a_{12} = -2.268 \times 10^{-3} \\
a_{21} = 2.696 \times 10^{-3}, & a_{22} = -0.02 \\
b_{11} = 3.772 \times 10^{-3}, & b_{12} = 0.157 \\
b_{21} = 3.772 \times 10^{-3}, & b_{22} = 13.483
\]

(27)

Therefore, the two critical transfer functions in (24) and (25) are as follows and plotted in Fig. 5.

\[
H_c(s) = \frac{4.012(s + 12.306)}{(s + 7.6)(s + 20.01)}
\]

(28)

\[
H_d(s) = \frac{14344(s + 6.638)}{(s + 7.6)(s + 20.01)}
\]

(29)

### A. Controller Design

In order to obtain tight output voltage regulation, a voltage mode controller is employed and designed according to the control to output transfer function in Fig. 5b. The block diagram of the closed-loop system is depicted as Fig. 6. The output voltage is first attenuated by overall sensor gain \( G_c(s) \) with 1/40 which includes the gain of differential amplifier (2.5) and the output voltage sensing resistor (1/100).

From the control point of view, an integrator with a DC gain is required to eliminate the steady-state error and adding a zero at 19.297, corresponding to 3.1 Hz, for speeding up the transient response. In this paper, PWM controller TL494 is utilized for output voltage regulation. However, different from ordinary feedback configuration in text book [29], the PI compensator in the TL494 is designed with the following transfer function and shown in Fig. 7.

\[
G_c(s) = \frac{10.75(s + 19.297)}{s}
\]

(30)

Hence, the loop gain of the overall system is

\[
T(s) = k_{PWM}G_c(s)G_e(s)H_d(s) = \frac{1.1k(s + 6.638)(s + 23.8)}{(s + 7.6)(s + 20.01)}
\]

(31)
Figure 5: Bode plots of (a) line to output and (b) control to output transfer functions at 220 Vrms

Figure 6: Block diagram of closed-loop system in voltage mode control

Figure 7: PI compensator design in TL494

where $k_{PWM}$ is the PWM modulator gain and defined as $1/V_p$, $V_p$ denotes the peak value of the modulation signal used in PWM, $1/3.5 ~V^{-1}$.

As a result, the Bode plot of the overall loop gain is depicted in Fig. 8. Its bandwidth and phase margin are 107 Hz and 90° respectively.

Figs. 9 and 10 show the waveforms of the line input voltage along with its current under full load condition at 110 Vrms and 220 Vrms input voltage respectively. In addition, the measured current harmonics met the IEC61000-3-2 class D standard as shown in Fig. 11.

The proposed converter can achieve fast and tight regulation of output voltage either in line input or load disturbances shown in Figs. 12 and 13 respectively. It can be seen that the output variation is about 1% of output voltage and settling time is about 40ms. Note that to maintain the output voltage without low frequency ripple, a substantial output capacitor is required.

Fig. 14 illustrates that the maximum measured efficiency in universal line input is 89.5%. At 150 Vrms point, the full load efficiency can be higher than that in the low line input even
using higher switching frequency. Figs. 15 and 16 show that, by utilizing higher switching frequency at high line input, the circuit efficiency has been increased by 1% and its averaged duty cycle can be extended by at least 4% (all above 0.1).

Based on the circuit parameters and (6) in [27], the voltage conversion ratio ($V_B/V_{in,pk}$) against inductance ratio $M$ ($L_2/L_1$) has been plotted in Fig. 17. In addition, the calculated and measured intermediate bus voltage $V_B$ under universal line input at light load condition were recorded in Fig. 18. The measured bus voltage $V_B$ shows the same trend as that of the predicted value and keeping well below 400 V. Fig. 19 experimentally proves that voltage stress on the bus capacitor is below 400 V at all conditions. Therefore, a DC bus capacitor rated 400 V instead of 450 V could be used.

**B. Comparison**

In order to compare with the existing converters [25] and [30], the two inductors and its ratio of the proposed circuit have to be changed for getting the same output voltage. Table II shows the components which were used in the comparison. From the table, we can see that the size of two inductors in the proposed circuit is the smallest among three converters. In addition, the operation mode utilized in the proposed converter...
is more robust with fixed frequency while the converters [30] and [25] are more sensitive to the noise because of zero current detection in the current return path. In addition, their variable frequency operation increases the difficulty in designing EMI filter.

Fig. 20 illustrates the conversion efficiency comparison between [25] and the proposed circuit. In addition, efficiency of the converter in [30] at 120 Vrms and 264 Vrms is 89.8% and 91.5% respectively. Due to the presence of the blocking diode in series with $L_1$ in the power stage and DCM operation of the proposed circuit, it has lower efficiency than that of [25] but nearly the same as [30]. Also, the minimum switching frequency in [25] is 20 kHz which is lower than the proposed circuit by 5 times but with the price of larger inductance which is also about 5 times larger than in the proposed circuit. However, the efficiency in the proposed circuit operating at fixed frequency also can achieve above 89% over the entire range of universal line input. It should be noted that using higher switching frequency at high line in this case isn’t suitable, where the averaged duty cycle is about 10%, because the switching losses become significant and slightly impair the efficiency of the converter.

Table II: Circuit Parameters Comparison

<table>
<thead>
<tr>
<th></th>
<th>$L_1$</th>
<th>$L_2$</th>
<th>Sensing output voltage</th>
<th>Operation Mode</th>
<th>Power Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prop.</td>
<td>142 uH</td>
<td>53.4 uH</td>
<td>Required</td>
<td>DCM (fixed frequency)</td>
<td>0.981 @120 Vrms 0.927 @270 Vrms</td>
</tr>
<tr>
<td>[25]</td>
<td>740 uH</td>
<td>250 uH</td>
<td>Required</td>
<td>BCM (variable frequency)</td>
<td>0.998 @120 Vrms 0.968 @270 Vrms</td>
</tr>
<tr>
<td>[30]</td>
<td>853 uH</td>
<td>662.5 uH</td>
<td>Not Required</td>
<td>BCM (variable frequency)</td>
<td>0.990 @120 Vrms 0.924 @264 Vrms</td>
</tr>
</tbody>
</table>

Table III: Inductors Comparison

<table>
<thead>
<tr>
<th></th>
<th>$L_1$</th>
<th>$L_2$</th>
<th>Core</th>
<th>Effective Volume</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prop.</td>
<td>142 uH</td>
<td>53.4 uH</td>
<td>$L_1$: RM4</td>
<td>$L_1$: 318mm$^3$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$L_2$: RM4</td>
<td>$L_2$: 318mm$^3$</td>
</tr>
<tr>
<td>[25]</td>
<td>740 uH</td>
<td>250 uH</td>
<td>$L_1$: RM6</td>
<td>$L_1$: 1050mm$^3$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$L_2$: RM5</td>
<td>$L_2$: 530mm$^3$</td>
</tr>
<tr>
<td>[30]</td>
<td>853 uH</td>
<td>662.5 uH</td>
<td>$L_1$: RM6</td>
<td>$L_1$: 1050mm$^3$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$L_2$: RM6</td>
<td>$L_2$: 1050mm$^3$</td>
</tr>
</tbody>
</table>
V. CONCLUSION

An integrated Boost Buck-Boost (IBoBuBo) single-stage AC/DC converter has been experimentally verified and the results showed the voltage stress on the bus capacitor can be kept well below 400 V in universal line input at all conditions. For the universal line input operation, it gives reliable performance without getting efficiency penalty at high line input. The tight output voltage regulation as well as high power factor can be achieved. Extended analysis of the proposed circuit and design of the controller have also been given and verified. In addition, the size and cost of the proposed circuit is reduced compared with the isolated single-stage solutions owning to absence of snubber, demagnetizing circuits and transformer. Employing higher switching frequency and working in DCM achieve smaller size of inductors and result in higher power density with compatible efficiency. The conversion efficiency of the proposed converter, thanks to the direct power transfer, reaches above 85% at full load condition 100 V output for all line input voltages.

APPENDIX

Figure 21: Power flow graph of the proposed converter

Fig. 7 in [27] is redrawn as Fig. 21. By equating the input and output power of the PFC cell, the average duty cycle $d_1$ can be obtained.

$$P_{in} = P_{o,PFC} = V_T I_{o,PFC}$$  
(32)

$$I_{o,PFC} = \frac{V_T}{R_{L&PFC} + R_{DC/DC&PFC}}$$  
(33)

where $V_T$ is the output voltage of PFC cell which is $V_o + V_B$ and $I_{o,PFC}$ is denoted the output current from the PFC cell. $R_{L&PFC}$ and $R_{DC/DC&PFC}$ are the equivalent resistances of the output load and DC/DC cell looking from the PFC cell respectively.

All the equations (9), (12)-(14) in [27] will also be used in the derivation. Due to lossless operation, the output power from the PFC cell equals the load power. Therefore,

$$P_{in} = \frac{d_1^2 V_{in,pk}^2}{2\pi L_1 f_S} \int_0^\pi \frac{\sin^2 \theta}{V_T - V_{in,pk} \sin \theta} d\theta$$  
(34)

$P_{dir,PFC} = n P_{o,PFC}$  
(35)

$$P_{o,DC/DC} = (1 - n) P_{o,PFC}$$  
(36)

$$\frac{P_{dir,PFC}}{P_{o,PFC}} = \frac{V_o}{V_T} = n$$  
(37)

where $n$ is the power ratio that the portion of input power can be delivered to output directly.

From (37), it gives

$$P_{dir,PFC} = n P_{o,PFC}$$  
(38)

Similarly, the equivalent resistance of DC/DC cell from the view of PFC cell can be obtained

$$R_{DC/DC&PFC} = \frac{R_{DC/DC}}{1 - n} = \frac{V_B^2}{(1 - n) P_o}$$  
(39)

where $R_L$ and $R_{DC/DC}$ are the output load and resistance of DC/DC cell respectively.

Putting (34), (38) and (39) into (32), the averaged duty cycle can be yielded

$$P_{in} = \frac{V_T^2}{R_{L&PFC} + R_{DC/DC&PFC}}$$  
(40)

$$d_1^2 V_{in,pk}^2 \int_0^\pi \frac{\sin^2 \theta}{V_T - V_{in,pk} \sin \theta} d\theta = \frac{R_L}{n} + \frac{V_B^2}{(1 - n) P_o}$$  
(41)

REFERENCES


